(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 678 849 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **95400894.2**

(51) Int. Cl.[6] : **G09G 3/36**

(22) Date of filing : **21.04.95**

(30) Priority : **22.04.94 JP 107599/94**

(43) Date of publication of application :
25.10.95 Bulletin 95/43

(84) Designated Contracting States :
DE FR GB

(71) Applicant : **SONY CORPORATION**
7-35 Kitashinagawa 6-chome
Shinagawa-ku
Tokyo 141 (JP)

(72) Inventor : **Meakawa, Toshikazu**
c/o Sony Corporation,
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)
Inventor : **Uchino, Katsuhide**
c/o Sony Corporation,
7-35, Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)

(74) Representative : **Thévenet, Jean-Bruno et al**
Cabinet Beau de Loménie
158, rue de l'Université
F-75340 Paris Cédex 07 (FR)

(54) Active matrix display device with precharging circuit and its driving method.

(57) To restrict an oscillation in the potential of a video line, caused by a high speed sampling rate, the active matrix display device is comprised of gate lines X forming rows, signal lines Y forming columns and liquid crystal pixels LC of the matrix arranged at crossing points of both lines. A V driver 1 scans in sequence each of the gate lines X and selects the liquid crystal pixels LC of one line for a corresponding horizontal period. The H driver 4 performs a sampling of the video signal VSIG for each of the signal lines Y and performs a writing of the video signal VSIG in the liquid crystal pixels LC the row selected during the corresponding horizontal period. Precharging means 5 supplies a predetermined precharging signal VPS to each of the signal lines Y just before writing the video signal VSIG for the liquid crystal pixels LC in one row. With such an arrangement as above, it is possible to reduce the charging or discharging amount in each of the signal lines Y when the video signal VSIG is sampled and further to restrict the oscillation of the potential in the video line 2.

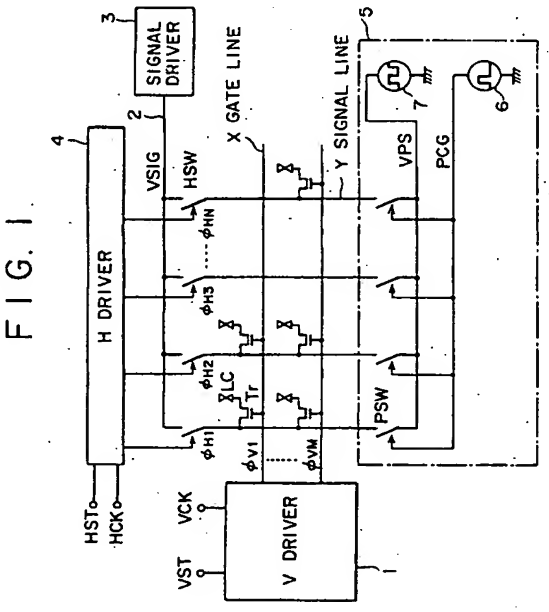


FIG. 1

EP 0 678 849 A1

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an active matrix display device and its driving method. More particularly, this invention relates to a technology for restricting the oscillation in the potential of a video line which accompany high-speed scanning of signal lines.

Description of Related Art

Referring now to Fig. 7, a configuration of the prior art active matrix display device will be described in brief. As shown, the active matrix display device is comprised of gate lines X (constituting rows) and signal lines Y (constituting columns). Pixels of the matrix are arranged at crossing points of the gate and signal lines. Each of the pixels is comprised, for example, of liquid crystal cells LC and thin film transistors Tr for driving the cells. In addition, this device has a V driver (a vertical scanning circuit) 101, by means of which each of the gate lines X is scanned in sequence so that the pixels of one row are selected for a respective horizontal period. In addition, this device has a horizontal scanning circuit by means of which video signals VSIG are sampled in respect to each of the signal lines Y and then the video signals VSIG are written into the pixels of the row selected for the corresponding horizontal period. This horizontal scanning circuit is comprised of horizontal switches HSW arranged at an end part of each of the signal lines Y, and H drivers 102 for controlling them in sequence for turning them on or off. Each of the signal lines Y is connected to the video line through the aforesaid horizontal switches HSW. The aforesaid video signals VSIG are supplied from the signal driver 103 to the video line. In order to control each of the horizontal switches HSW for its turning on or off in sequence, the H driver 102 outputs horizontal sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ... ϕ_{HN}.

Fig. 8 represents waveforms of sampling pulses ϕ_{H1}, ϕ_{H2}, and ϕ_{H3} outputted in sequence from the H driver 102 shown in Fig. 7. As the active matrix display device is made to be highly accurate in operation and the number of pixels is remarkably increased, the sampling rate is correspondingly made fast. As a result, a width τ_H of each of the sampling pulses is disturbed. As the sampling pulses are applied to their corresponding horizontal switches HSW, the video signals VSIG supplied from the video line are sampled at each of the signal lines Y through the conducting HSW. Since each of the signal lines Y has a predetermined capacitance, a charging or a discharging is produced at the signal lines Y in response to the sampling pulses, thereby a potential in the video line is caused to oscillate. As described above, in the case where the sampling rate is made fast, a pulse width of each of the sampling pulses is disturbed, a charging or a discharging amount is not constant and the potential in the video line is caused to vary. Thus, there occurs a problem that this potential variation is caused to overlap with the video signals VSIG, some vertical stripes are produced in the displayed image and the quality of image is deteriorated.

In the case of video signals in accordance with the normal NTSC standards, the sampling rate is relatively low and a next sampling pulse occurs after the potential oscillation in the video line has stopped, so that the influence of the oscillation of potential is reduced. However, in the case of HDTV driving or a double-speed NTSC driving, the sampling rate is remarkably increased and so it is difficult to make an effective restriction on the oscillation of potential in the video line. In general, the sampling pulses supplied to HSW are produced by an H driver composed of shift registers constructed by thin film transistors (TFT). A TFT has a lower mobility or has a larger disturbance in physical constants as compared with a normal transistor made of monolithic silicon, so that it is difficult to perform a precision control over the sampling pulses produced by this circuit. In addition to this disturbance in sampling pulse width, the ON resistance in HSW has a certain disturbance, so that there may occur a certain variation in charging or discharging characteristic in the signal lines. Due to this fact, the potential in the video line is caused to oscillate, this state is caused to overlap with the actual video signal to cause appearance of vertical stripes, resulting in a significant deterioration in the quality of the displayed image.

SUMMARY OF THE INVENTION

In view of the aforesaid technical problems found in the prior art, it is an object of the present invention to restrict oscillation in the potential of the video line generated as the sampling rate of the video signal is increased. In order to accomplish the aforesaid object, the present invention has provided the following means. That is, the active matrix display device of the present invention is provided with gate lines constituting rows, signal lines constituting columns and matrix pixels arranged at crossing points of both lines, as its basic configuration. In addition, there are also provided a vertical scanning circuit in which each of the gate lines is scanned in sequence and pixels in each row are selected for a corresponding respective horizontal period and a horizontal scanning circuit in which the video signals are sampled at each of the signal lines and the video signals are written on the pixels in the row selected within one horizontal period. As a feature of the present invention, there is provided a precharging means and predetermined precharging signals are supplied to each of the signal lines just prior to the writing of the video signals in respect to the pixels in the selected row.

The precharging means supplies a precharging signal having a grey level with respect to the video signal varying between the white level and the black level. Alternatively, in the case that an AC reverse driving is to be carried out, the precharging means supplies the precharging signal similarly reversed for every one horizontal period in order to cause its polarity to be coincided with the video signal reversed for every one horizontal period.

In accordance with one preferred embodiment of the present invention, the precharging means is separately arranged from the horizontal scanning circuit and is comprised of a plurality of switching elements connected to an end part of each of the signal lines, and a control means for totally turning on or off each of the switching elements and applying a precharging signal to each of the signal lines. In accordance with another preferred embodiment of the present invention, the precharging means is arranged integral with the horizontal scanning circuit and is comprised of a plurality of switching elements connected to an end part of each of the signal lines, and a control means for turning on or off in sequence each of switching elements during writing operation, sampling the video signals to the corresponding signal line and, in turn, totally turning on or off each of the switching elements just before writing and applying the precharging signal included in the video signal to each of the signal lines.

The present invention includes a method for driving the active matrix display device. This driving method performs a vertical scanning for scanning in sequence each of the gate lines and selecting pixels in a respective one row for each one horizontal period, a horizontal scanning for sampling in sequence the video signals in respect to each of the signal lines and writing the video signals into the pixels in the row selected during the respective one horizontal period, and a precharging for totally supplying the predetermined precharging signals to each of the signal lines just before writing the video signals to the pixels in the one row.

According to the present invention, all the signal lines are precharged in advance up to a potential near the video signals at a timing not influencing the displaying operation. With such an arrangement as above, a charging or discharging amount when the actual video signals are sampled at each of the signal lines is reduced and a potential oscillation at the video line is restricted.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram for showing the first preferred embodiment of the active matrix display device of the present invention.

Fig. 2 is a timing chart applied for illustrating an operation in the first preferred embodiment.

Fig. 3 is a circuit diagram for showing the second preferred embodiment of the active matrix display device of the present invention.

Fig. 4 is a timing chart applied for illustrating an operation of the second preferred embodiment.

Fig. 5 is a block diagram for showing one example of a synthesizing circuit of video signals used in the second preferred embodiment.

Fig. 6 is also a timing chart to be applied for illustrating an operation in the second preferred embodiment.

Fig. 7 is a block diagram for showing one example of the prior art active matrix display device.

Fig. 8 is a waveform figure to be applied for illustrating the problem in the prior art active matrix display device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings, the preferred embodiments of the present invention will be described in detail. Fig. 1 is a schematic circuit diagram for showing the first preferred embodiment of the active matrix display device of the present invention. As shown in the figure, the active matrix display device is comprised of gate lines X forming rows and signal lines Y forming columns arranged in a matrix. There are provided liquid crystal pixels LC arranged at each of the crossing points of the gate lines X and the signal lines Y. Although the active matrix display device of the present preferred embodiment is provided with some liquid crystal pixels, it is of course apparent that it may be provided with other pixels of electro-optical substances. The liquid crystal pixels LC are driven by thin film transistors Tr. Source electrodes of the thin film transistors Tr are connected to the corresponding signal lines Y, gate electrodes are connected to the corresponding gate lines X and drain electrodes are connected to the corresponding liquid crystal pixels LC.

V driver 1 is connected to each of the gate lines X so as to constitute the vertical scanning circuit. This V driver 1 transfers vertical start signals VST in sequence in response to a predetermined clock signal VCK and supplies selection pulses ϕ_{V1}, ... ϕ_{VM} to each of the gate lines X. With such an arrangement as above, each of the gate lines X is scanned in sequence and the liquid crystal pixels LC in one respective row are selected for each one horizontal period.

In turn, respective signal lines Y are connected to the video line 2 through corresponding horizontal switching elements HSW. To the video line 2 are supplied the video signals VSIG from the signal driver 3. In addition, there is provided an H driver 4 so as to control turning on or off of each of the horizontal switching elements HSW. That is, the H driver 4 transfers in sequence the horizontal start signals HST in

synchronism with the predetermined horizontal clock signal HCK and outputs the sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ϕ_{H4}, ... ϕ_{HN} so as to turn on or off the horizontal switching elements HSW. The horizontal scanning circuit is constituted by the H driver 4 and the horizontal switching elements HSW, the video signals VSIG are sampled in respect to each of the signal lines Y, and the video signals VSIG are written through the thin film transistors Tr kept conductive with respect to the pixels LC in the row selected within one horizontal period.

As a feature of the present invention, there is provided a precharging means 5 by means of which a predetermined precharging signal VPS is supplied to each of the signal lines Y just prior to writing of the video signals VSIG in the liquid crystal pixels LC in one row, and then a charging or a discharging amount of each of the signal lines Y generated when the video signals VSIG are sampled is reduced. In the preferred embodiment above, the precharging means 5 is separately arranged from the aforesaid horizontal scanning circuit, and is comprised of a plurality of switching elements PSW connected to the end part of each of the signal lines Y, and a control means 6 for totally turning on or off each of the switching elements PSW and applying the precharging signals VPS to each of the signal lines Y. In the preferred embodiment, this control means 6 outputs a control pulse PCG. In addition, the precharging signal VPS is supplied from the signal source 7 separately arranged from the signal driver. This precharging signal VPS has a grey level with respect to the video signals VSIG varying between the white level and the black level. In the preferred embodiment, although the horizontal switching elements HSW and the additional switching elements PSW are arranged at both ends of the signal lines Y, the present invention is not limited to this arrangement, but PSW may be arranged at the same side as HSW.

Now, referring to the timing chart of Fig. 2, operation of the active matrix display device shown in Fig. 1 will be described in detail. The vertical clock signal VCK inputted to the V driver 1 has a pulse width corresponding to one horizontal period (1H). In addition, the control pulse PCG outputted from the control means 6 is outputted within a horizontal non-effective period such as a horizontal blanking period, for example. If the control pulse PCG overlaps the horizontal effective period, there is a possibility that the precharging signals VPS will be written into the liquid crystal pixels. In addition, when the selection pulses ϕV outputted in sequence from the V driver 1 shown in Fig. 1 are overlapped and the control pulse PCG is outputted during that period, the precharging signal VPS is similarly apt to be written into the liquid crystal pixels and so it is necessary to prevent this phenomenon. Then, the horizontal start pulses HST supplied to the H driver 4 are outputted just after the selection pulses PCG for every one horizontal period, and then the sampling of the video signals VSIG is started. This sampling is carried out in sequence in synchronism with the horizontal clock signal HCK supplied to the H driver 4.

Here, the video signal VSIG supplied from the signal driver 3 through the video line 2 has a reverse polarity for every one horizontal period, so an AC driving is being carried out. In response to this operation, the precharging signal VPS supplied from the signal source 7 is also reversed for every one horizontal period and has its polarity coincided with that of the video signals VSIG. The precharging signal VPS has a potential level of Vp corresponding to a central potential of the video signal VSIG and just expresses a grey level positioned between the white level and the black level. In this way, the potential level of the precharging signal VPS in the preferred embodiment is basically set to a grey level in which its uniformity can be most visually discriminated. The last waveform in the timing chart of Fig. 2 represents the potential VY applied to a respective signal line Y. When the control signal PCG is outputted at the initial stage of one horizontal period and an additional switching element PSW is made conductive, the precharging signals VPS are applied to all the signal lines Y and then the charging or discharging is carried out for a capacitance component. Applying of this precharging signal VPS causes the potential VY in each of the signal lines Y to become a level of Vp. After this operation, the actual video signal VSIG is sampled in respect to each of the signal lines Y, its potential VY is changed in response to VSIG and writing is carried out. A potential variation ΔV caused by the writing operation is reduced to VSIG - Vp and thus the charging or discharging amount is reduced. As described above, the present invention employs a constitution in which all the signal lines Y are precharged in advance up to a potential of middle level at a timing such as the horizontal blanking period not applying any influence to the displayed video, the charging or discharging current in the signal line generated when the actual video signal VSIG is sampled, and thus a potential oscillation in the video line 2, is restricted. In other words, the charging or discharging of each of the signal lines Y is almost finished through the additional switching element PSW, and the charging or discharging with the actual video signal VSIG is produced only with a difference between the potential levels of the precharging signal VPS and the video signal VSIG.

Fig. 3 is a circuit diagram for showing the second preferred embodiment of the active matrix display device of the present invention. Each of the crossing points between the gate lines X and the signal lines Y is provided with the liquid crystal pixels LC and the thin film transistors Tr for driving the pixels. To each of the gate lines X are connected the V drivers 11 so as to constitute the vertical scanning circuit.

In turn, each of the signal lines Y is connected to the video line 12 through the horizontal switching elements HSW comprised of transmission gates. To the video line 12 are supplied the video signals Vsig. The video signals Vsig are processed in such a manner that they include a precharging signal part at a pre-processing stage. To each of the horizontal switching elements HSW is connected a respective NAND gate through a delay circuit DLY composed of a combination of five inverters. To one input terminal of each of the NAND gates is applied a signal A outputted from each of the stages of the H shift register 13. To the other input terminal of each NAND gate is applied a blanking signal PRG through an inverter IVT. The horizontal scanning circuit is comprised of the H shift register 13, NAND gates, delay circuits DLY and horizontal switching elements HSW and the like.

In this second preferred embodiment, the precharging means is integrally arranged with the horizontal scanning circuit, wherein the horizontal switching elements HSW connected to the end part of each of the signal lines Y are utilized. In addition, NAND gates are used as control means, each of the switching elements HSW is turned on or off in sequence during a writing operation, the video signals Vsig are sampled in the corresponding signal lines Y and in turn each of the switching elements HSW is totally turned on or off just before the writing operation so as to apply the precharging signal contained in a part of the video signal Vsig to each of the signal lines Y.

In the preferred embodiment of the present invention, the vertical scanning circuit for scanning the gate lines linearly in sequence and selecting pixels in one row for every horizontal period has been employed, although another vertical scanning circuit for selecting two or more rows concurrently may be applied. In addition, a point sequential process in which video signals are supplied in sequence to each of the signal lines through the horizontal switching elements has been described, although this process can be applied to another system in which the video signals are written by line-at-a-time scanning into the signal lines.

Before starting description of the operation of the active matrix display device shown in Fig. 3, referring now to Fig. 4, a pre-processing of the video signals will be described. As shown, the original video signals VSIG are divided into the actual video period and the blanking period for every one horizontal period. The video signals VSIG reverse in synchronism with the reversing signals FRP for every one horizontal period. The video signals VSIG are processed in synchronism with the blanking signals PRG and then the precharging signals having predetermined potential levels V_{P1} and V_{P2} are inserted within the blanking period. The video signal Vsig synthesized in this way is indicated at the lowest stage in the timing chart of Fig. 4.

Referring now to Fig. 5, one example of a circuit configuration for performing a pre-processing of the video signals is shown. As shown in this figure, this circuit has a resistor dividing part 21, wherein a power supply voltage Vdd-Vss is divided by resistance value to produce two voltage levels V_{P1} and V_{P2}. One voltage level V_{P1} is supplied to an H input of the analog switch 22, the other voltage level V_{P2} is supplied to an L input. This analog switch 22 applies the reversed signal FRP as a selection input, selects V_{P1} and V_{P2} alternately for every one horizontal period and outputs it. The values V_{P1}, V_{P2} selected in this way are supplied to one input of the next stage analog switch 23. To the other input of the analog switch 23 are supplied the original video signals VSIG. The analog switch 23 alternatively inserts V_{P1}, V_{P2} for every one horizontal period within the blanking period with the blanking signal PRG being applied as a select input and then outputs the synthesized video signal Vsig.

Lastly, referring now to Fig. 6, an operation of the active matrix display device shown in Fig. 3 will be described in detail. As illustrated in this figure, the synthesized video signal Vsig has alternatively the voltage levels V_{P1}, V_{P2} for every one horizontal period within the blanking period and shows a waveform including the precharging signal.

The H shift register 13 shown in Fig. 3 outputs the sampling pulses A1, A2, A3, ... AN for every stage through a respective inverter IVT. In addition, NAND gates arranged for each stage produce the drive pulses D1, D2, D3, ... DN with reference to the sampling pulse and the blanking signal PRG. The drive pulses are similarly supplied to the corresponding switching element HSW through the delay circuit DLY arranged for each stage so as to turn it on or turn it off.

As indicated in the timing chart of Fig. 6, the drive pulses D1, D2, D3, ... DN have leading pulses which are synchronous with the blanking period. With such an arrangement as above, each of the horizontal switching elements HSW is totally turned on or off and the potential level V_{P2} or V_{P1} of the precharging signal included in the synthesized video signal Vsig is applied to each of the signal lines. Accordingly, the potentials VY1, VY2, ... VYN in each of the signal lines are once charged to the level of V_{P2}. In addition, at the leading end of the next horizontal period, it is charged to the potential level V_{P1} of the opposite polarity. After this blanking period has elapsed, each of the drive pulses D1, D2, D3, ... DN controls again in sequence to turn on or turn off HSW and performs a sampling of the actual video signals. In this way, all HSWs are once made conductive within the blanking period, precharging signal levels (V_{P1}, V_{P2}) are written in each of the signal lines Y and held just before the actual video signals are written. That is, the charging or discharging in each of the signal lines Y within the blanking period is almost finished and the charging or discharging when the actual video signals are sampled is operated only for the difference ΔV between the

precharging signal level and the actual video signal level. With the above operation, a potential oscillation (noise) in the video line is restricted and it becomes possible to remove the fixed pattern of the vertical stripes.

As described above, according to the present invention, the charging or discharging amount at each of the signal lines is reduced when the video signals are sampled by supplying the predetermined precharging signal to each of the signal lines just before writing the video signals for the pixels in one row. With such an operation as above, noise in the video line generated through charging or discharging of the video signals is substantially reduced, so that the present invention can obtain some effects that the fixed pattern of vertical stripes can be removed and video quality can be substantially improved. In addition, since it is not necessary to consider a slight disturbance in sampling pulse outputted from the horizontal scanning circuit, the present invention provides an effect that the circuit design margin can be reduced. For a similar reason, since it is possible to reduce the power supply voltage in the horizontal scanning circuit, the present invention may provide an effect that a consumption power can be reduced. In particular, the present invention may provide some effects that the precharging can be realized only through including the precharging signal in the video signals and controlling of the sampling operation in the horizontal scanning circuit and no burden in circuit design may occur.

Claims

1. An active matrix display device comprising :
   a plurality of gate lines (X) arranged in rows;
   a plurality of signal lines (Y) arranged in columns;
   pixels arranged at each of crossing points of said gate lines and signal lines;
   a vertical scanning circuit (1) for line-at-a-time scanning each of the gate lines and selecting pixels of at least one row;
   a horizontal scanning circuit (HSW,4) for sampling video signals (VSIG) in sequence and writing the video signals in sequence in pixels in the selected row(s); and
   a precharging circuit (5) for supplying a precharging signal (VPS) to each of the signal lines just before writing the video signals with respect to pixels of one row.

2. An active matrix display device according to claim 1 in which supplying of said precharging signals is carried out at once for all signal lines.

3. An active matrix display device according to claim 1 in which said precharging circuit supplies a precharging signal (VPS) having a grey level in respect to a video signal varying between a white level and a black level.

4. An active matrix display device according to claim 1 in which said precharging circuit (5) supplies a precharging signal inverted for every one horizontal period in such a way that its polarity is coincided with that of a video signal (VCK) inverted for every one horizontal period.

5. An active matrix display device according to claim 1 in which said precharging circuit (5) is provided with a plurality of switching elements (PSW) connected to an end part of each of the signal lines, and with a control circuit (6) for turning on or off at once each of the switching elements and applying the precharging signal to each of the signal lines.

6. An active matrix display device according to claim 5 in which said control circuit (6) outputs a control pulse (PCG) within a horizontal non-effective period.

7. An active matrix display device according to claim 6 in which said horizontal non-effective period is a horizontal blanking period.

8. An active matrix display device according to claim 1 in which said precharging circuit (5) is arranged at opposite side or same side of said horizontal scanning circuit.

9. An active matrix display device according to claim 1 in which said precharging circuit is integrally arranged with said horizontal scanning circuit and includes a plurality of switching elements (HSW) connected to an end part of each of the signal lines and a control circuit (13) for turning on or off in sequence each of the switching elements during writing operation, sampling a video signal in a corresponding signal line, and in turn, at once turning on or off each of the switching elements just before a writing operation and applying the precharging signal contained at a part of the video signal to each of the signal lines.

10. A method for driving an active matrix display device including a plurality of gate lines (X) arranged in row, a plurality of signal lines (Y) arranged in column and pixels arranged at crossing parts between said gate lines and signal lines comprising the steps of :
    line-at-a time scanning each of the gate lines (X) and selecting pixels in at least one row;

sampling video signals (VSIG) in sequence and writing the video signals in the pixels in the selected row; and

providing a predetermined precharging signal (VPS) to each of the signal lines just before writing the video signals in respect to pixels in one row.

11. A method for driving an active matrix display device according to claim 10 in which said precharging signals (VPS) are supplied simultaneously to said signal lines.

12. A method for driving an active matrix display device according to claim 10 in which said video signals are written by dot sequential scanning.

13. A method for driving an active matrix display device according to claim 10 in which said video signals are written by line-at-a-time scanning.

FIG. 1

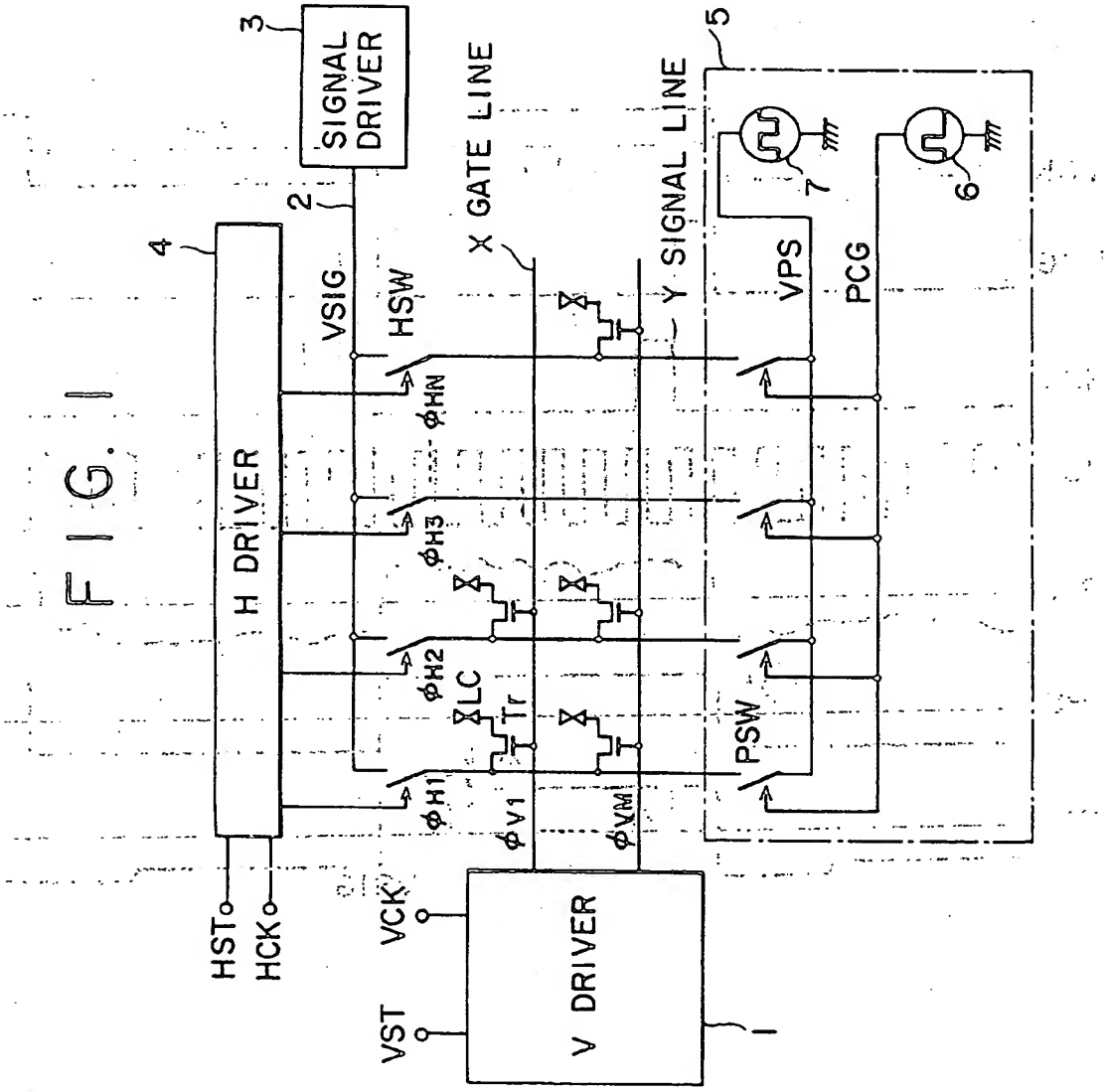

3
SIGNAL DRIVER
2
4
H DRIVER
VSIG
HSW
X GATE LINE
Y SIGNAL LINE
5
VPS
PCG
7
6
φHN
φH3
φH2
LC
Tr
φH1
φV1
φVM
PSW
HST
HCK
VCK
VST
V DRIVER
1

FIG. 2

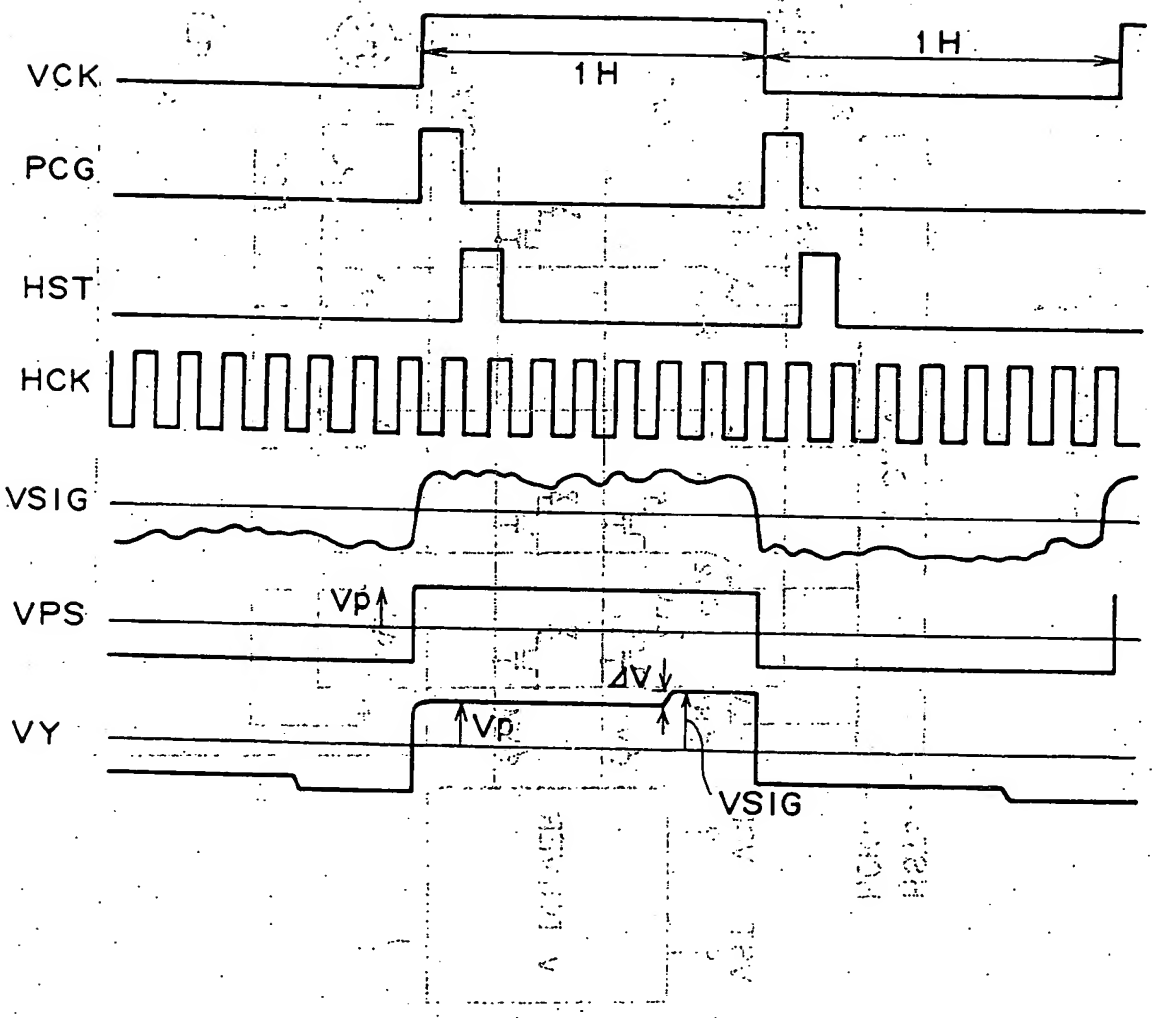


FIG. 3

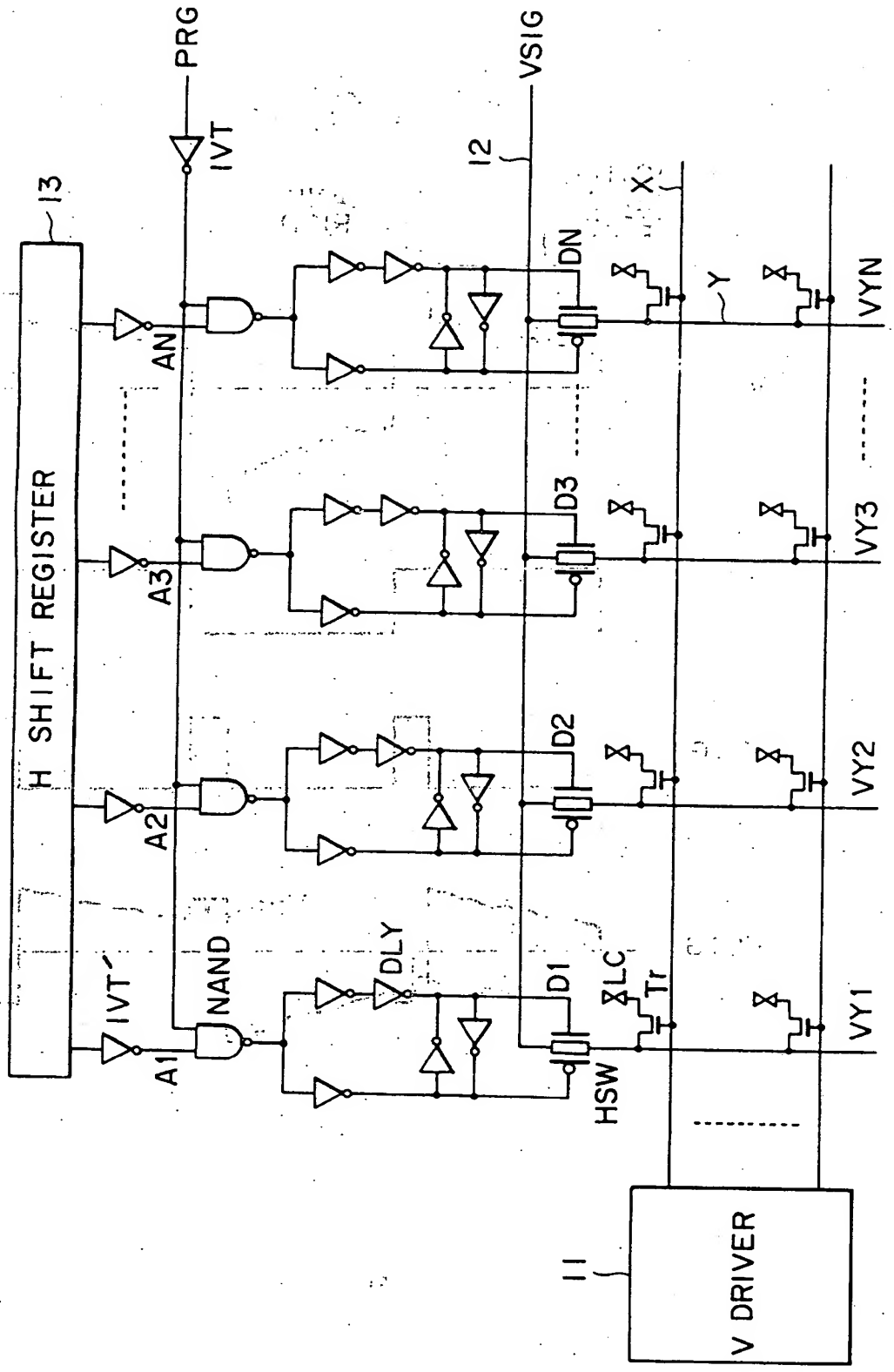

PRG
IVT
VSIG
13
12
X
H SHIFT REGISTER
AN
A3
A2
A1
IVT'
NAND
DLY
DN
D3
D2
D1
HSW
LC
Tr
Y
VYN
VY3
VY2
VY1
11
V DRIVER

FIG. 4

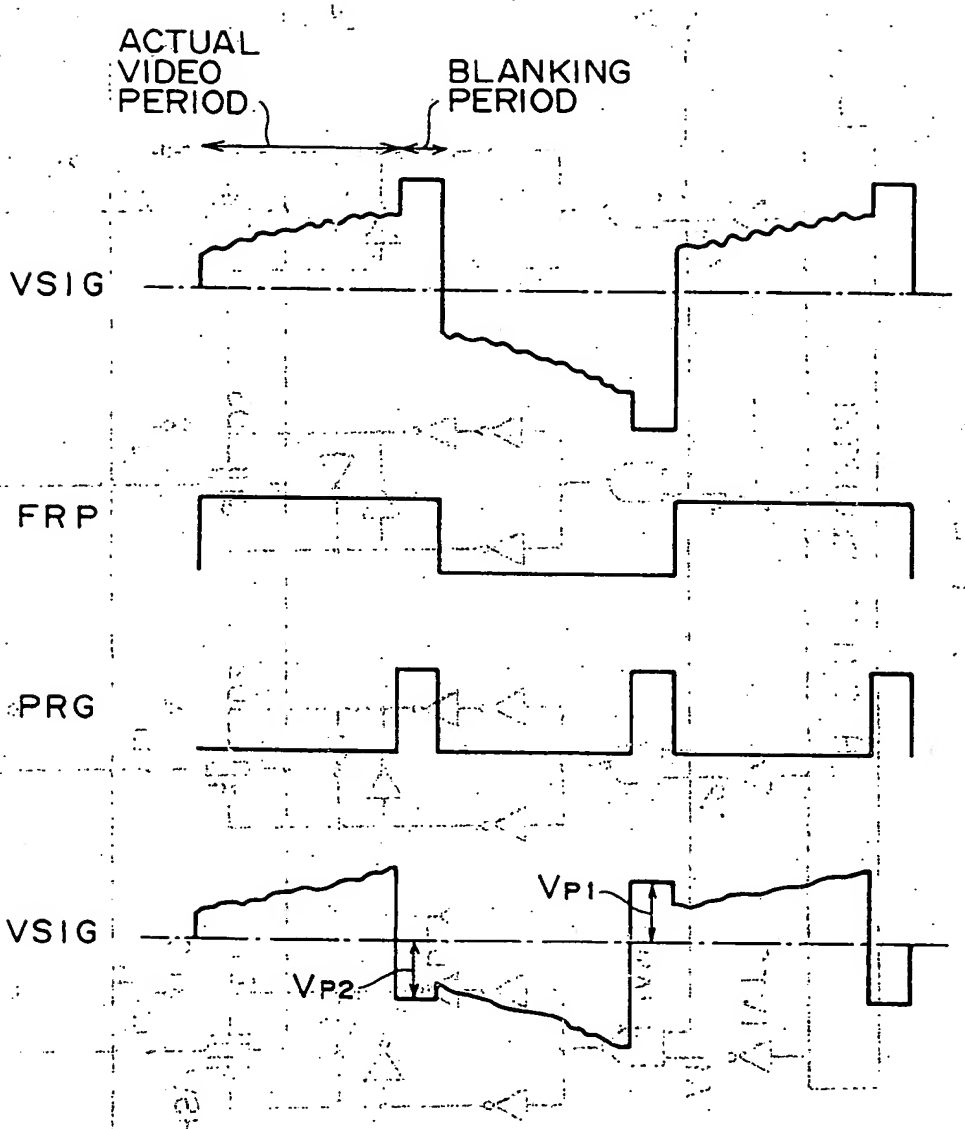


FIG. 5

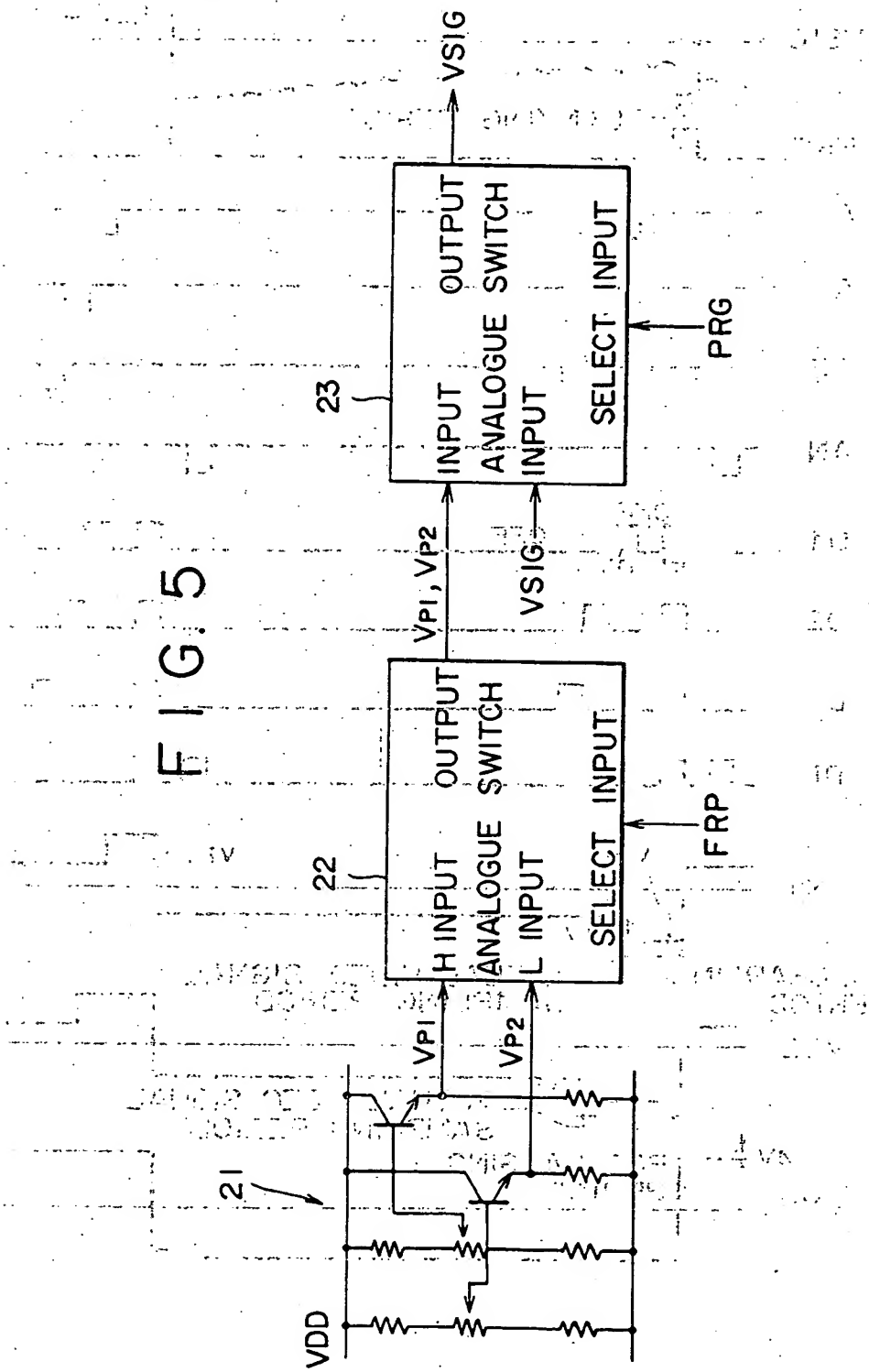

VSIG
OUTPUT
ANALOGUE SWITCH
INPUT
SELECT INPUT
PRG
23
VP1, VP2
VSIG
OUTPUT
ANALOGUE SWITCH
H INPUT
L INPUT
SELECT INPUT
FRP
22
VP1
VP2
21
VDD

FIG. 6

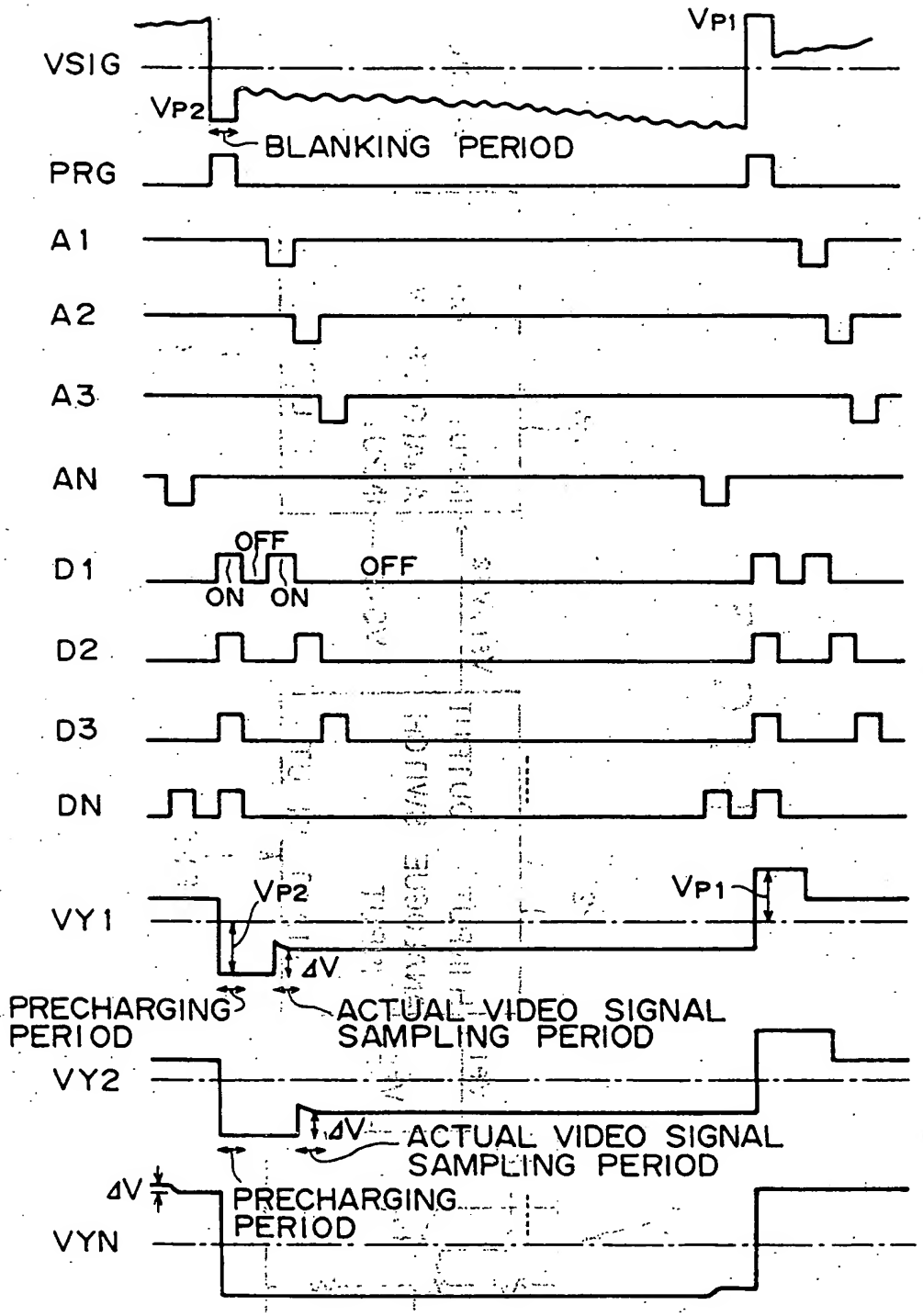


FIG. 7

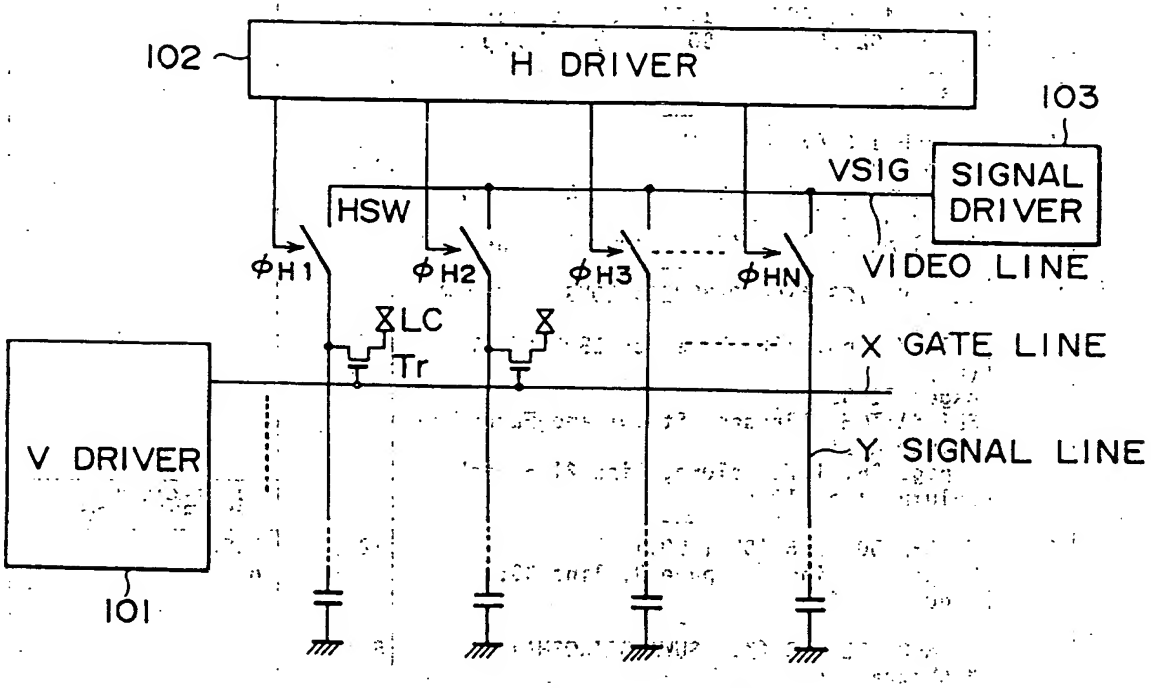
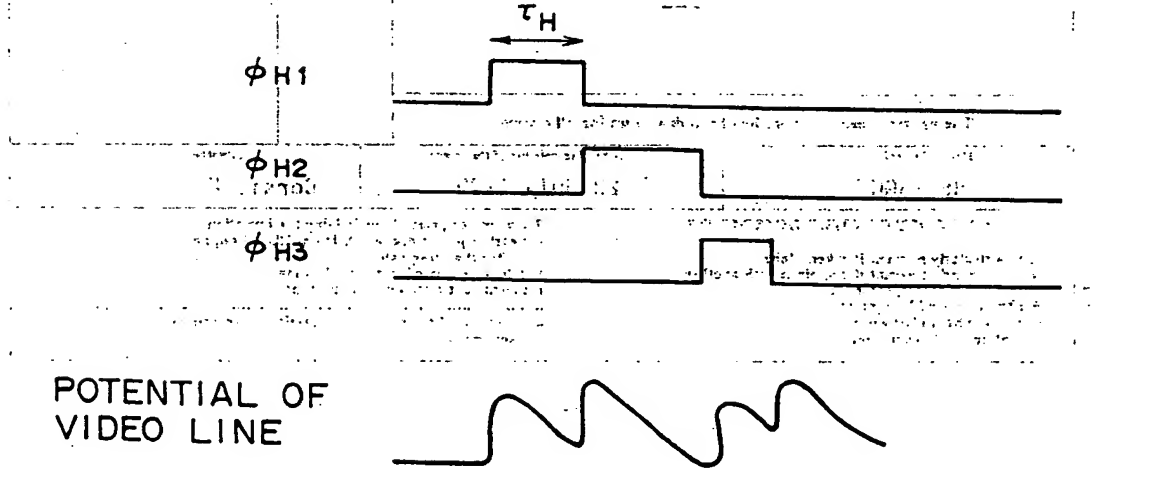

102
H DRIVER
103
VSIG
SIGNAL DRIVER
HSW
φH1
φH2
φH3
φHN
VIDEO LINE
LC
Tr
X GATE LINE
V DRIVER
Y SIGNAL LINE
101

FIG. 8


τH
φH1
φH2
φH3
POTENTIAL OF VIDEO LINE

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 40 0894

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	PATENT ABSTRACTS OF JAPAN vol. 14 no. 498 (P-1124) ,30 October 1990 & JP-A-02 204718 (SONY CO.) 14 August 1990, * abstract *	1,2,5-8, 10,11 9,12,13	G09G3/36
Y A	US-A-5 166 671 (MAEKAWA) * Abstract * * column 1, line 18 - column 3, line 21; figures 1-4C * * column 5, line 47 - column 6, line 56 *	13 1,10	
Y	ELECTRONICS AND COMMUNICATIONS IN JAPAN PT.2, vol. 76, no. 112, December 1993 NEW YORK (US), pages 31-39, SEI SAITOH 'Present Status and Future of Driver LSI' * page 36, left column, line 21 - right column, line 14 *	9	
Y	FR-A-2 507 366 (SONY CO.) * page 5, line 7 - page 9, line 33; figures 1-4H *	12	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G09G H04N
A	GB-A-2 081 018 (K.K.SUWA SEIKOSHA) * Abstract * * page 6, column 48 - column 94; figures 15-17 *	8,12	
P,X	WO-A-94 10676 (YUEN FONG YU H.K. CO. LTD.) * Abstract * * page 6, line 24 - page 11, line 18; figures 1-5 * * page 12, line 1 - page 14, line 2 *	1-3,5,6, 8-11,13	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 July 1995	Corsi, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)